WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate comprising a first region extending along an edge and a second region surrounded by the first region;

a plurality of memory cell arrays provided in the second region, and comprising a plurality of cells having an MTJ element;

a plurality of gate transistors provided in the first region, and having a current path having a first terminal connected with a bit line, which is a signal read path from the cells, and a second terminal opposite to the first terminal;

a plurality of data buses connected with a same number of the second terminals;

a connection control circuit provided in the first region, and connected with an end of the data buses, and connecting selected two of the data buses to first and second output terminals, respectively; and

an amplifier circuit provided in the first region, and amplifying a potential difference in accordance with signals outputted from the first and second output terminals.

2. The device according to claim 1, wherein the memory cell array has no transistor other than a select transistor that the cells have.

3. The device according to claim 1, wherein the cells include:

a plurality of memory cells storing data; and

a plurality of reference cells storing reference data used for determining the data.

4. The device according to claim 3, wherein the gate transistors include:

a plurality of data gate transistors connected with bit lines, which are signal read paths from the memory cells; and

a plurality of reference data gate transistors connected with reference bit lines, which are signal read paths from the reference cells.

5. The device according to claim 4, wherein the reference data gate transistors are connected to the data buses.

6. The device according to claim 5, wherein

the reference cells include a first reference cell storing data "0" and a second reference cell storing data "1" and

the connection control circuit connects one of the data buses selectively connected with the first reference cell and one of the data buses selectively connected with the second reference cell to the first output terminal, and connects one of the data buses selectively connected with a first memory cell of the memory cells to the second output terminal.

7. The device according to claim 6, wherein the amplifier circuit includes a clamping circuit section, which clamps signals supplied from the first and second output terminals to a predetermined potential in accordance with the signals.

8. The device according to claim 6, wherein

the connection control circuit further includes a third output terminal, and connects one of the data buses selectively connected with the second memory cell selected by the same address as the first memory cell to the third output terminal, and

the amplifier circuit has a first section amplifying a potential difference in accordance with signals outputted from the first and second output terminals, and a second section amplifying a potential difference in accordance with signals outputted from the first and third output terminals.

9. The device according to claim 8, wherein the amplifier circuit further includes a clamping circuit section, which is provided in the first region and clamps signals supplied from the first to third output terminals to a predetermined potential in accordance with the signals.

10. The device according to claim 8, wherein the connection control circuit includes a clamping circuit section, which clamps signals supplied from the data buses to a predetermined potential in accordance with

the signals.

11. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of memory cell arrays provided in a center of the semiconductor substrate, and comprising a plurality of cells having an MTJ element; and

a plurality of peripheral functional sections provided only around the memory cell arrays on the semiconductor substrate, at least one of the peripheral functional sections including:

a plurality of gate transistors having a current path having a first terminal connected with one bit line, which is a signal read path from the cells, and a second terminal opposite to the first terminal;

a plurality of data buses connected with a same number of the second terminals;

a connection control circuit connected with an end of the data buses, and connecting selected two of the data buses to first and second output terminals, respectively; and

an amplifier circuit amplifying a potential difference in accordance with signals outputted from the first and second output terminals.

12. The device according to claim 11, wherein the memory cell array has no transistor other than a select transistor that the cells have.

13. The device according to claim 11, wherein the cells include:

a plurality of memory cells storing data; and

a plurality of reference cells storing reference data used for determining the data.

14. The device according to claim 13, wherein the gate transistors include:

a plurality of data gate transistors connected with bit lines, which are signal read paths from the memory cells; and

a plurality of reference data gate transistors connected with reference bit lines, which are signal read paths from the reference cells.

15. The device according to claim 14, wherein the reference data gate transistors are connected to the data buses.

16. The device according to claim 15, wherein

the reference cells include a first reference cell storing data "0" and a second reference cell storing data "1" and

the connection control circuit connects one of the data buses selectively connected with the first reference cell and one of the data buses selectively connected with the second reference cell to the first output terminal, and connects one of the data buses selectively connected with a first memory cell of the memory cells to the second output

terminal.

17. The device according to claim 16, wherein the amplifier circuit includes a clamping circuit section, which clamps signals supplied from the first and second output terminals to a predetermined potential in accordance with the signals.

18. The device according to claim 16, wherein

the connection control circuit further includes a third output terminal, and connects one of the data buses selectively connected with the second memory cell selected by the same address as the first memory cell to the third output terminal, and

the amplifier circuit has a first section amplifying a potential difference in accordance with signals outputted from the first and second output terminals, and a second section amplifying a potential difference in accordance with signals outputted from the first and third output terminals.

19. The device according to claim 18, wherein the amplifier circuit further includes a clamping circuit section, which is provided in the first region and clamps signals supplied from the first to third output terminals to a predetermined potential in accordance with the signals.

20. The device according to claim 18, wherein the connection control circuit includes a clamping circuit section, which clamps signals supplied from the data

buses to a predetermined potential in accordance with the signals.